LMK03318 Ultra-Low Jitter Clock Generator Family with One PLL, Eight Outputs, Integrated EEPROM

1 Features

- Ultra Low Noise, High Performance
  - Jitter: 100 fs RMS typical, Fout > 100 MHz
  - PSRR: -70 dBc, robust supply noise immunity
- Flexible Device Options
  - Up to 8 AC-LVPECL, AC-LVDS, AC-CML, HCSL or LVCMOS outputs or any combination
  - Pin mode, I^2C mode, EEPROM mode
  - 71 pin selectable pre-programmed default startup options
- Dual Inputs with automatic or manual selection
  - Crystal input: 10 to 52 MHz
  - External input: 1 to 300 MHz
- Frequency Margining Options
  - Fine frequency margining using low-cost pullable crystal reference
  - Glitchless coarse frequency margining (%) using output dividers
- Other Features
  - Supply: 3.3 V core, 1.8/2.5/3.3 V output supply
  - Industrial temperature range (-40ºC to +85ºC)
  - Package: 7 mm x 7 mm 48-QFN

2 Applications

- Switches & Routers
- Network & Telecom Line Cards
- Servers & Storage Systems
- Wireless Base Station

3 Description

The LMK03318 is an ultra-low-noise clock generator with one fractional-N frequency synthesizer with integrated VCO, flexible clock distribution/fanout, and pin-selectable configuration states stored in on-chip EEPROM. The device can generate multiple clocks for various multi-gigabit serial interfaces and digital devices, reduces BOM cost and board area, and improves reliability by replacing multiple oscillators and clock distribution devices. The ultra-low-jitter reduces bit error rate (BER) in high-speed serial links.

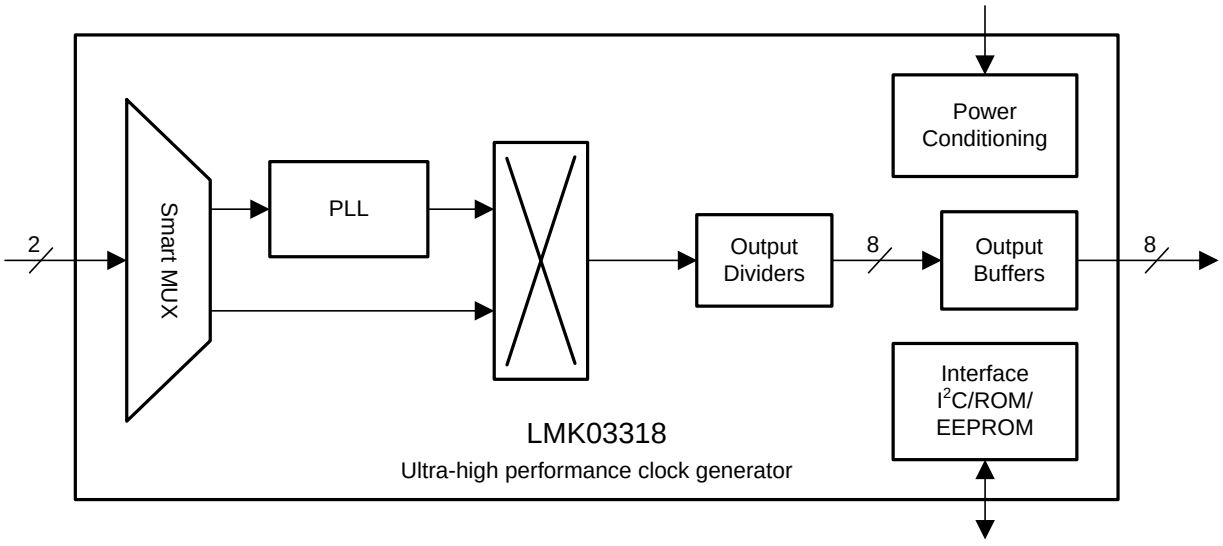
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK03318	48-QFN	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PRODUCT PREVIEW

LMK03318 Simplified Block Diagram



4 Description Continued

For the PLL, a differential/single-ended clock or crystal input can be selected as its reference clock. The selected reference input can be used to lock the VCO frequency at an integer or fractional multiple of the reference input frequency. The VCO frequency can be tuned between 4.8 GHz and 5.4 GHz. The PLL offers the flexibility to select a predefined or user-defined loop bandwidth, depending on the needs of the application. The PLL has a post-divider that can be selected between divide-by 2, 3, 4, 5, 6, 7 or 8.

All the output channels can select the divided-down VCO clock from the PLL as the source for the output divider to set the final output frequency. Some output channels can also independently select the reference input for the PLL as an alternative source to be bypassed to the corresponding output buffers. The 8-bit output dividers support a divide range of 1 to 256 (even or odd), output frequencies up to 1 GHz, and output phase synchronization capability.

All output pairs are ground-referenced CML drivers with programmable swing that can be interfaced to LVDS, LVPECL or CML receivers with AC coupling. All output pairs can also be independently configured as HCSL outputs or 2x 1.8-V LVCMOS outputs. The outputs offer lower power at 1.8 V, higher performance and power supply noise immunity, and lower EMI compared to voltage-referenced driver designs (such as traditional LVDS and LVPECL drivers). Two additional 3.3-V LVCMOS outputs can be obtained via the STATUS pins. This is an optional feature in case of a need for 3.3-V LVCMOS outputs and device status signals are not needed.

The device features self startup from on-chip programmable EEPROM or pre-defined ROM memory, which offers multiple custom device modes selectable via pin control eliminating the need for serial programming. The device registers and on-chip EEPROM settings are fully programmable via I^2C-compatible serial interface. The device slave address is programmable in EEPROM and LSBs can be set with a 3-state pin.

The device provides two frequency margining options with glitch-free operation to support system design verification tests (DVT), such as standard compliance and system timing margin testing. Fine frequency margining (in ppm) can be supported by using a low-cost pullable crystal on the internal crystal oscillator (XO), and selecting this input as the reference to the PLL synthesizer. The frequency margining range is determined by the crystal's trim sensitivity and the on-chip varactor range. XO frequency margining can be controlled through pin or I^2C control for ease-of use and high flexibility. Coarse frequency margining (in %) is available on any output channel by changing the output divide value via I^2C interface, which synchronously stops and restarts the output clock to prevent a glitch or runt pulse when the divider is changed.

Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The analog and digital core blocks operate from 3.3 V ± 5% supply and output blocks operate from 1.8 V / 2.5 V / 3.3 V ± 5% supply.

5 Device and Documentation Support

5.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

5.2 Trademarks

E2E is a trademark of Texas Instruments.

5.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK03318RHSR	PREVIEW	WQFN	RHS	48	2500	TBD	Call TI	Call TI	-40 to 85		
LMK03318RHST	PREVIEW	WQFN	RHS	48	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

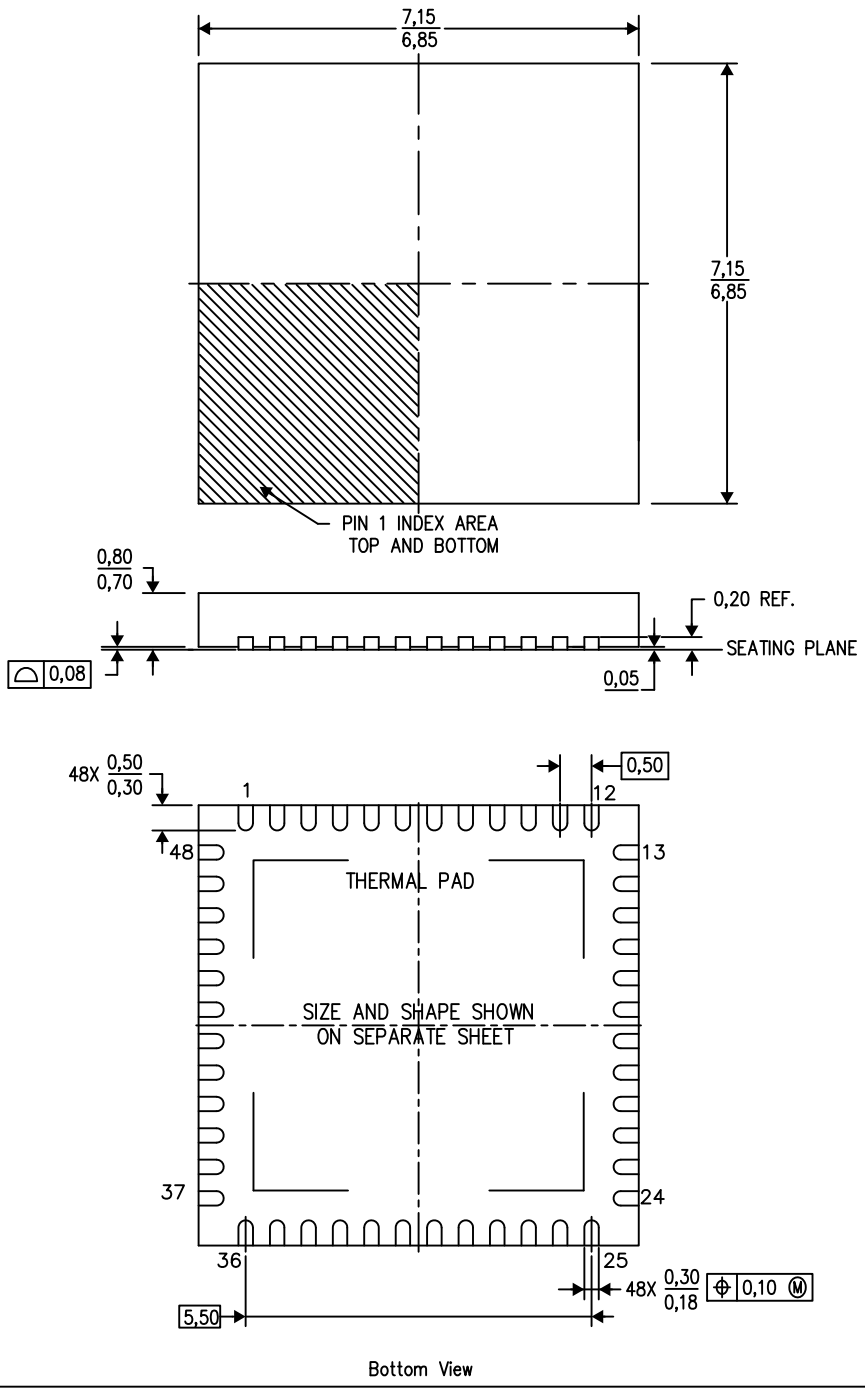
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHS (S–PWQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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